LRCC68 Long-Range LoRa Wireless Transceiver Module

LoRa@ Wireless Module-Powered by Semtech

DataSheet

V1.1

Table of Contents

1 Overview

1.1 Description

The LRCC68 is a low-cost, ultra-low-power, and ultra-compact LoRa® RF module, based on the high-performance Semtech LLCC68 LoRa® wireless communication IC. It supports LoRa and LoRaWAN frequencies ranging from 868 MHz to 915 MHz and primarily utilizes the next-generation LoRa™ modulation technology for ultra-long-range spread spectrum communication.

The LRCC68 module is equipped with a high-quality TCXO, ensuring stable operation in industrial environments with extreme temperatures. Designed specifically for wireless sensor networks and other IoT devices, it is particularly suitable for applications requiring battery power, low power consumption, and long-range connectivity. The module features an SPI interface, allowing users to achieve wireless data transmission and reception by connecting it to an MCU via IO.

Note:
Since this module is a pure RF transceiver module, it requires the use of an MCU's SPI driver.

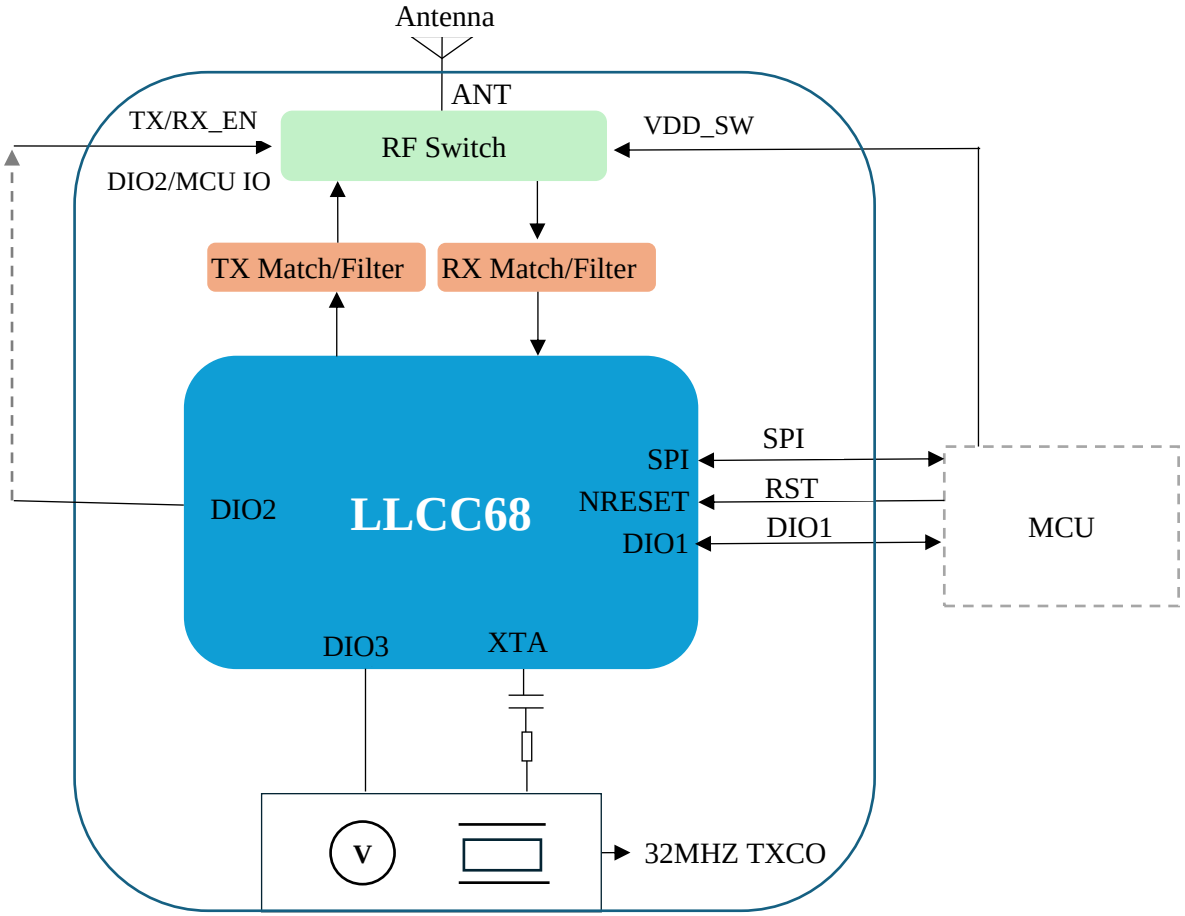
1.2 Features

- Compliant with LoRaWAN 1.0.3 standard specifications.
- Supported frequency bands: 868/915 MHz LoRa®/(G)FSK.
- LoRaWAN activation methods: Over-the-Air Activation (OTAA) and Activation by Personalization (ABP).
- Data rate (LoRa): 1.76-62.5 kbps
- LoRa point-to-point (P2P) communication.
- Temperature-compensated crystal oscillator (TCXO) utilized.
- Communication interface: Standard 4-wire SPI.
- Operating temperature range: -40°C to +85°C.
- Supply voltage: 1.8V to 3.7V.
- Low-power wireless system with bandwidth ranging from 7.81 kHz to 500 kHz/FSK.
- Supported spreading factors: SF5, SF6, SF7, SF8, SF9, SF10, SF11
- Low power consumption: 1.54 μA in sleep mode.
- LoRa power amplifier (PA) boost mode: Output power of 22 dBm in the Sub-GHz band.
- Module dimensions: 10 mm × 10 mm × 2.5 mm.
- Certifications: CE and FCC.

1.3 Applications

- IoT Node Communication
- Intelligent Parking Systems
- Intelligent Security Monitoring
- Smart Home Systems
- Intelligent Building Automation
- Agricultural Automation Monitoring
- Industrial Controllers and Sensors
- Smart Logistics
- Urban Management
- Healthcare and Medical Applications
- Long-Range Wireless Remote Control and Data Acquisition Systems

2 System Block Diagram



3 Hardware Overview

The hardware overview discusses the LRCC68 module interfaces, pin layout, and their corresponding pin functions.

3.1 Pin Layout

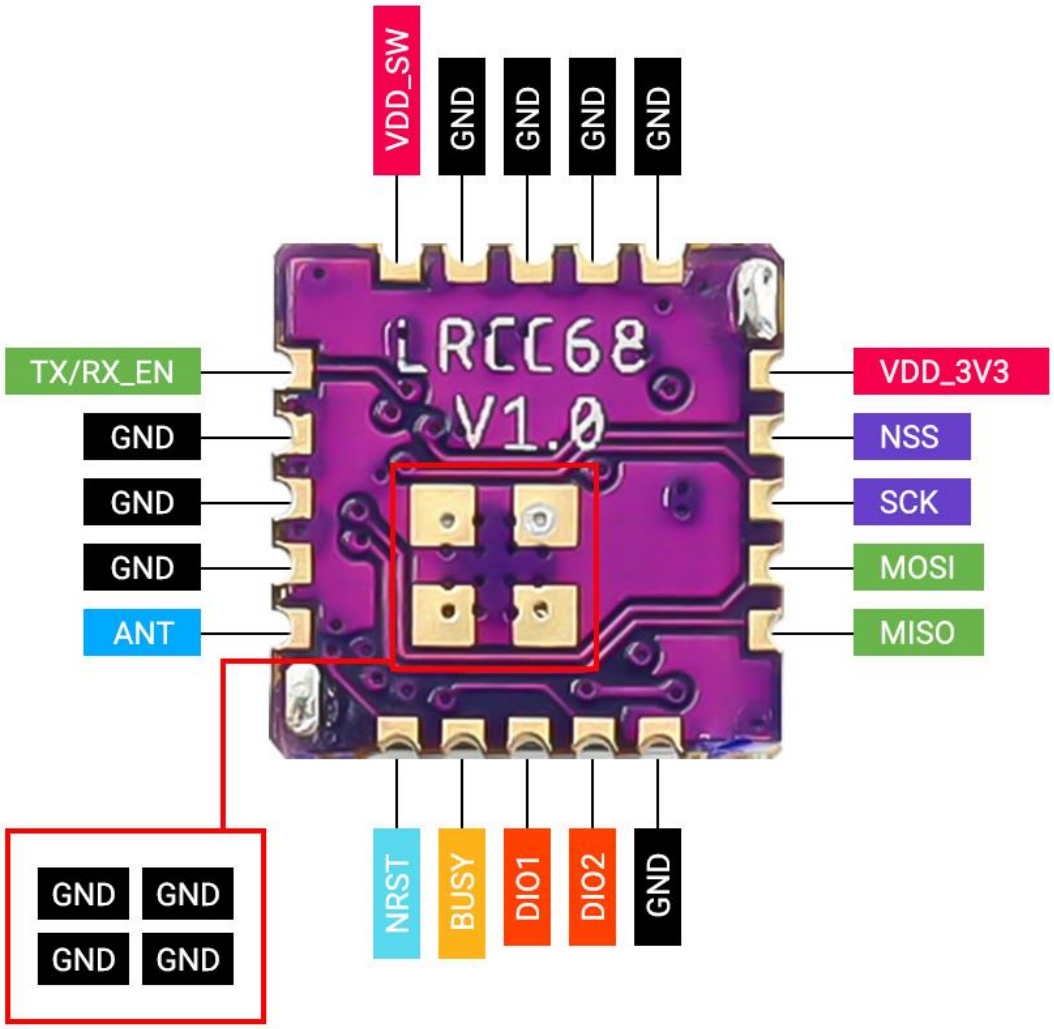


Figure 1:Pin Layout of the Module

3.2 Pin Definitions

The table below shows the module pin definitions and descriptions:

No.	Name	Type	Pin	Description
1	P$1	PWR	VDD_3V3	Power supply input
2	P$2	I	LR_NSS	SPI chip select input
3	P$3	I	LR_SCK	SPI clock input
4	P$4	I	LR_MOSI	SPI data input (Master Out Slave In)
5	P$5	O	LR_MISO	SPI data output (Master In Slave Out)
6	P$6	-	GND	Ground
7	P$7	I/O	LR_DIO2	The multi-purpose digital I/O, specifically DIO2 of the LLCC68 IC, can be connected to the TX/RX EN pin to serve as the control pin for the RF SPST (Single-Pole Single-Throw) switch.
8	P$8	I/O	LR_DIO1	Multi-purpose digital IO, connected to DIO1 of LLCC68
9	P$9	O	LR_BUSY	Internal status indicator pin
10	P$10	I	LR_NRESET	Reset pin to initialize the chip; low level to reset
11	P$11	AI/AO	ANT_LR	RF signal input/output port; use 50 Ω impedance matching for traces
12	P$12	-	GND	Ground
13	P$13	-	GND	Ground
14	P$14	-	GND	Ground
15	P$15	I	TX/RX_EN	RF enable control is connected to the external microcontroller's IO or DIO2. A high level indicates transmission, while a low level indicates reception.
16	P$16	I	VDD_SW	The RF switch power supply is high-level effective (1.8-3.3V). When entering low-power mode, VCC_SW must be set to a low level.
17	P$17	-	GND	Ground
18	P$18	-	GND	Ground
19	P$19	-	GND	Ground

20	P$20	-	GND	Ground
21	P$41	-	GND	Ground
22	P$42	-	GND	Ground
23	P$43	-	GND	Ground
24	P$44	-	GND	Ground

4 Module Specifications

No.	Item	Parameter	Specification	Unit
1	RF Characteristics	Main Chip	Semtech LLCC68	
2		LoRaWAN Frequency	Suitable for 868MHz (EU), 915MHz (US)	
3		Modulation Signal	LoRa®、（G）FSK	
4		LoRaWAN Protocol	LoRaWAN Protocol: Class A/B/C (Complies with LoRaWAN 1.0.3 Standard)	
5		Air Data Rate (LoRa)	1.76-62.5	Kbps
6		Transmission Power	+22（MAX）	dBm
7		Receiver Sensitivity	-125（TYP）	dBm
8	Packaging Type	Dimensions	10*10*2.5	mm
9		Packaging	24 pin Module, SMT Surface Mount	
10	Electrical Characteristics	Module Supply Voltage	3.3V@typical	V
11		TCXO Supply Mode	Through SX1262 DIO3	
12		TCXO Supply Voltage	1.8-3.3	V
13		Maximum Operating Current (Transmission)	120	mA
14		Maximum Operating Current (Reception)	7.5	mA
15		(Low Power) Sleep Current	1.54	uA
16	Other	TX/RX_EN	Transmission/Reception Enable Control	
17		SPI	SPI Communication Interface, including 4 pins	
18		LR_DIO1	Multi-purpose Digital IO, IC LLCC68's DIO1	
19		LR_DIO2	LR_DIO2: Multi-purpose Digital IO, IC LLCC68's DIO2, DIO2 connects TX/RX_EN to set the RF switch control pin	
20		LR_DIO3	LR_DIO3: DIO3 used as TCXO voltage supply	

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

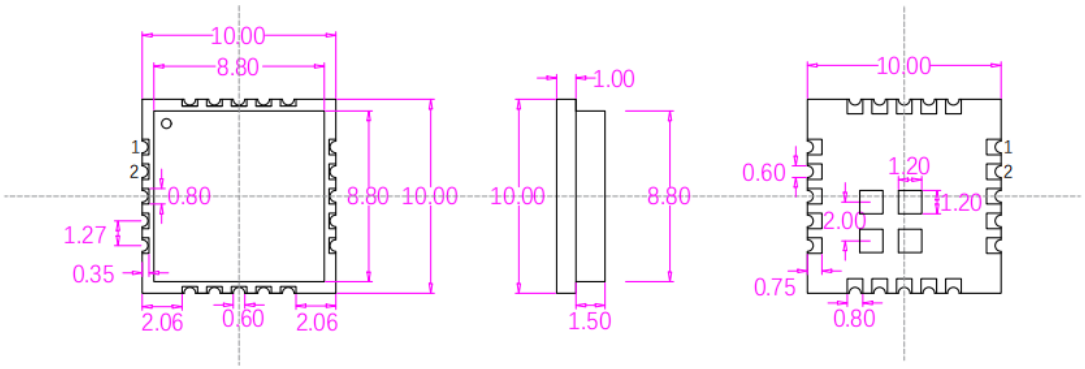
No.	Item	Description	Min	Max	Unit
1	V_{CC}	Supply Voltage	-0.5	3.9	V

5.2 Normal Operating Conditions

No.	Item	Description	Min	Typical	Max	Unit
1	V_{CC}	Supply Voltage	1.8	3.3	3.7	V
2	Top	Operating Temperature	-40	-	+85	° C

6 Mechanical Characteristics

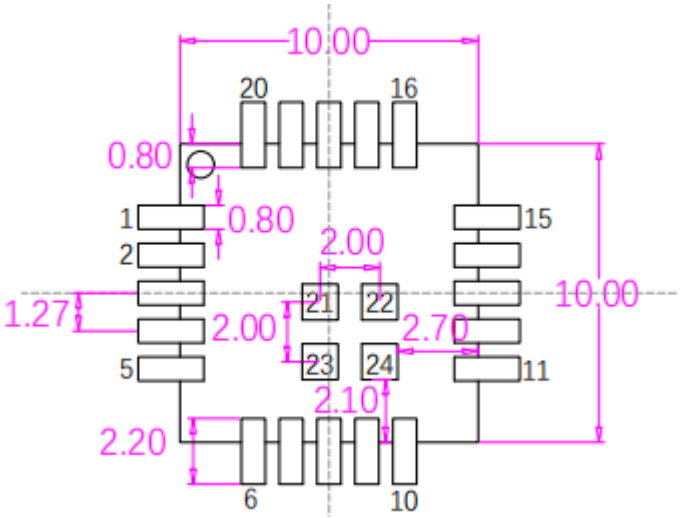
6.1 Module Dimensions



Top Side Bottom Unit:mm

Figure 2:Appearance Dimensions

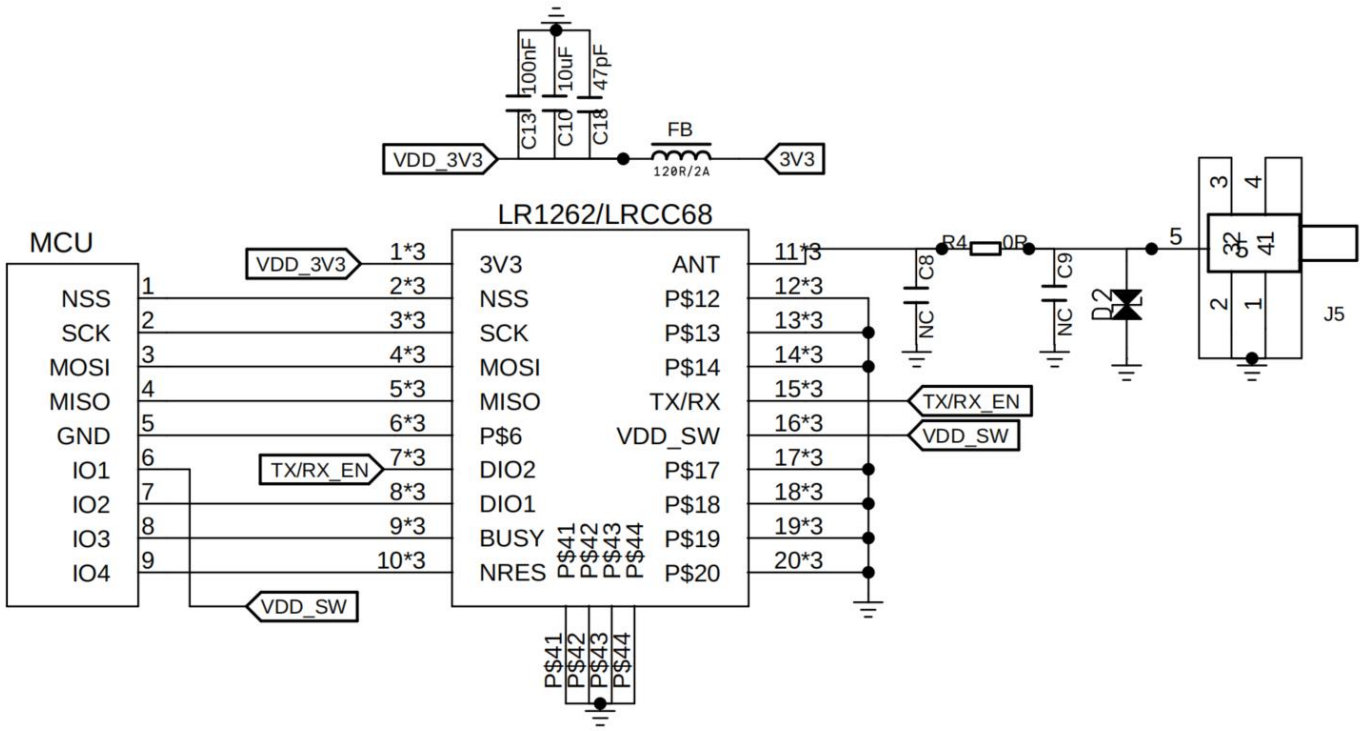
6.2 Layout Recommendations



Unit:mm

Figure 3:PCB Layout

6.3 Schematic Reference Design for Module



1. VDD_SW is the internal RF switch power supply pin, which is high-level effective (1.8-3.3V). A low level indicates the off state.

2. TX/RX_EN is the internal RF switch transmit/receive switching enable pin. When TX/RX_EN is connected to DIO2, the transmit/receive switching is controlled internally by the LR1262/LRCC68.

Figure 4: Schematic Reference Design

7 Certifications

8 Related Documents and Resources

- **LRCC68 Long-Range LoRa Wireless Transceiver Module Product Link**
- **LLCC68 Datasheet**

9 Revision History

Date	Version	Release Notes
2025/4/16	V1.0	Initial release
2025/6/20	V1.1	1 Revise the system block diagram 2 Modify the pin function definitions 3 Update the schematic reference design